What is claimed is:

1. An oscillator comprising a resonance circuit comprising:

a first series connected circuit having an inductive impedance element;

a second series connected circuit having a first capacitive impedance element, a first variable capacitive impedance element connected in series with said first capacitive impedance element and having a directional characteristic, and a second capacitive impedance element connected in series with said first variable capacitive impedance element; and

a third series connected circuit having a third capacitive impedance element, a second variable capacitive impedance element connected in series with said third capacitive impedance element and having a directional characteristic, and a fourth capacitive impedance element connected in series with said second variable capacitive impedance element, and

wherein said first series connected circuit, said second series connected circuit, and said third series connected circuit are connected in parallel, and said first variable capacitive impedance element and said second variable capacitive impedance element are oppositely connected with respect to either connection side of said second series connected circuit and said third series connected circuit, and

wherein variable capacities of said first variable capacitive impedance element and said second variable capacitive impedance element are externally controlled to be varied.

2. The oscillator according to claim 1, wherein the directional characteristic of said first variable capacitive impedance element and said second variable capacitive impedance element is a parasitic capacitance to ground, and one of the terminals of each of said first and second variable capacitive impedance elements which has a larger parasitic capacitance to ground is defined as a first terminal, while the other, which has a smaller parasitic capacitance to ground, is defined as a second terminal, and a first control voltage is applied to the first terminal of each of said first and second variable capacitive impedance elements, while a second control voltage is applied to the second terminal of each of said first and second variable capacitive impedance elements, said first control voltage and said second control voltage being adjusted to determine an oscillation frequency.

3. An oscillator comprising a resonance circuit comprising:

a first series connected circuit having an inductive impedance element;

a second series connected circuit having a first capacitive impedance element, a first variable capacitive impedance element connected in series with said first capacitive impedance element and having a predetermined directional characteristic, a second variable capacitive impedance element connected in series with and opposite said first variable capacitive impedance element, and a second capacitive impedance element connected in series with said second variable capacitive impedance element; and

a third series connected circuit having a third capacitive impedance element, a third variable capacitive impedance element connected in series with said third capacitive impedance element and having a predetermined directional characteristic, a fourth variable capacitive impedance element connected in series with and opposite said third variable capacitive impedance element, and a fourth capacitive impedance element connected in series with said fourth variable capacitive impedance element, and

wherein said first series connected circuit, said second series connected circuit, and said third series connected circuit are connected in parallel, and said second variable capacitive impedance element and said fourth variable capacitive impedance element are oppositely connected with respect to either connection side of said second series

connected circuit and said third series connected circuit, and

wherein one of the terminals of each of said first, second, third, and fourth variable capacitive impedance elements which has a larger value of said predetermined characteristic, is defined as a first terminal while the other, which has a smaller value of said predetermined characteristic, is defined as a second terminal, a first control voltage is applied to the first terminal of each of said first, second, third, and fourth variable capacitive impedance elements, while a second control voltage is applied to the second terminal of each of said first, second, third, and fourth variable capacitive impedance elements, said first control voltage and said second control voltage being adjusted to determine an oscillation frequency.

4. The oscillator according to claim 3, wherein the value of said predetermined characteristic is a parasitic capacitance to ground.

5. The oscillator according to claim 1, wherein said variable capacitive impedance element utilizes a gate capacity of a MOS transistor formed by a CMOS process.

6. A PLL circuit comprising:

an oscillator according to claim 2;

a charge pump to which a reference signal and an oscillation signal outputted by said oscillator are inputted and by which two output voltages are outputted in accordance with a difference in phase between said reference signal and said oscillation signal; and

a loop filter which low pass filters the two output voltages outputted by said charge pump, and

wherein, two outputs of said loop filter are connected to said oscillator so as to apply said first control voltage and said second control voltage to said oscillator.

7. A PLL circuit comprising:

an oscillator according to claim 2;

phase comparison means to which a reference signal and an oscillation signal outputted by said oscillator are inputted and by which two output voltages are outputted as an exclusive OR (XOR) of said reference signal and said oscillation signal and as a signal (XNOR) obtained by reversing said exclusive OR; and

a loop filter which low pass filters the two output voltages, and

two outputs of said loop filter are connected to said oscillator so as to apply said first control voltage and said second control voltage to said oscillator.

8. The PLL circuit according to claim 6 or 7, wherein one of the ends of each of a first and second switches is connected to a corresponding one of the two outputs of said loop filter, and the other end of each of said first and second switches is connected to a DC power source having a predetermined voltage.

9. The PLL circuit according to claim 6 or 7, wherein a reference voltage difference corresponding to a desired oscillation frequency is inputted to said oscillator using a desired timing.

10. The PLL circuit according to claim 6, wherein central voltage detecting means is connected to the two outputs of said loop filter to detect a central voltage between said first control voltage and said second control voltage, and a central voltage detection signal outputted by said central voltage detecting means is fed back to said charge pump.

11. The PLL circuit according to claim 6 or 7, wherein said loop filter has a first input terminal and a second input terminal to which the respective output voltages outputted by the charge pump are inputted, and a first output terminal and a second output terminal used to output said first control voltage and said second control voltage, respectively, to said

oscillator, and is configured so that an impedance from said first input terminal to said first output terminal is equal to an impedance from said second input terminal to said second output terminal, an impedance from said first input terminal to said second output terminal is equal to an impedance from said second input terminal to said first output terminal, and a floating capacity of the whole loop filter is balanced.

12. Communication equipment comprising a transmission circuit, a reception circuit, and an antenna, wherein said transmission and/or reception circuit has an oscillator according to claim 1 or a PLL circuit according to claim 6 or 7.

13. An oscillating method using an oscillation circuit comprising a resonance circuit comprising:

a first series connected circuit having an inductive impedance element;

a second series connected circuit having a first capacitive impedance element, a first variable capacitive impedance element connected in series with said first capacitive impedance element and having a directional characteristic, and a second capacitive impedance element connected in series with said first variable capacitive impedance element; and

a third series connected circuit having a third capacitive impedance element, a second variable capacitive impedance element connected in series with said third capacitive impedance element and having a directional characteristic, and a fourth capacitive impedance element connected in series with said second variable capacitive impedance element, and

wherein said first series connected circuit, said second series connected circuit, and said third series connected circuit are connected in parallel, and said first variable capacitive impedance element and said second variable capacitive impedance element are oppositely connected with respect to either connection side of said second series connected circuit and said third series connected circuit, and

wherein variable capacities of said first variable capacitive impedance element and said second variable capacitive impedance element are externally controlled to be varied.